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FIG. 1a

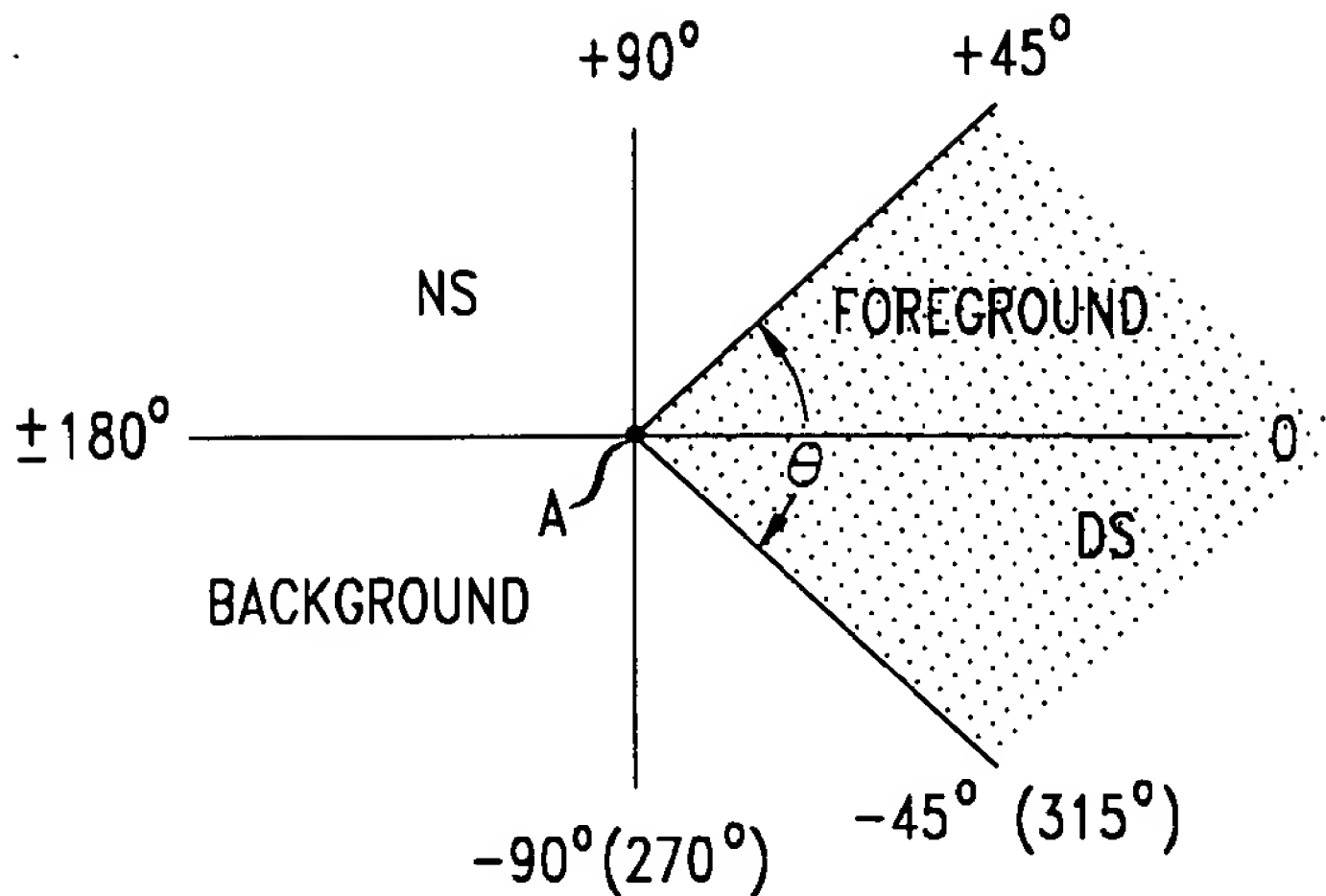


FIG. 1b

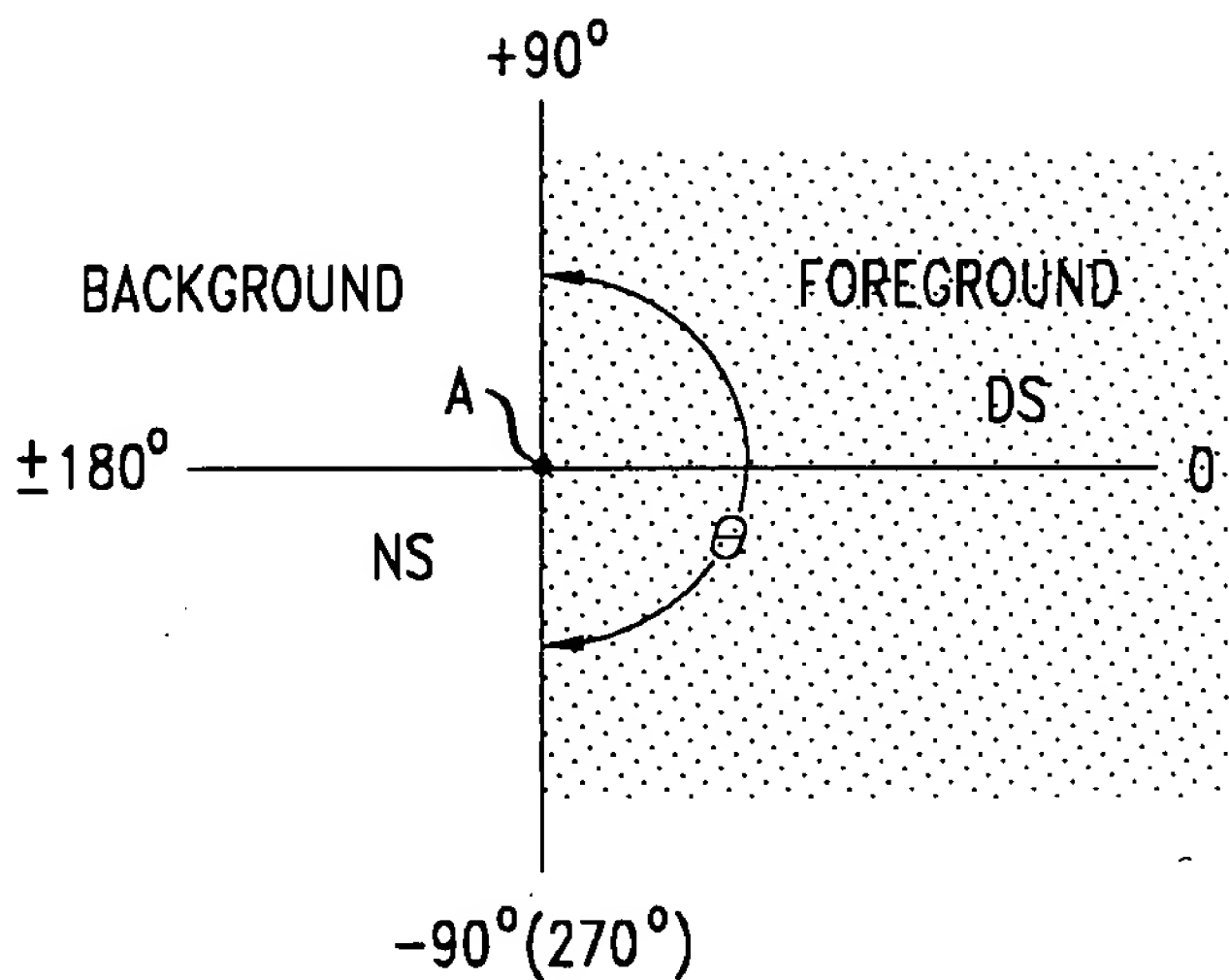
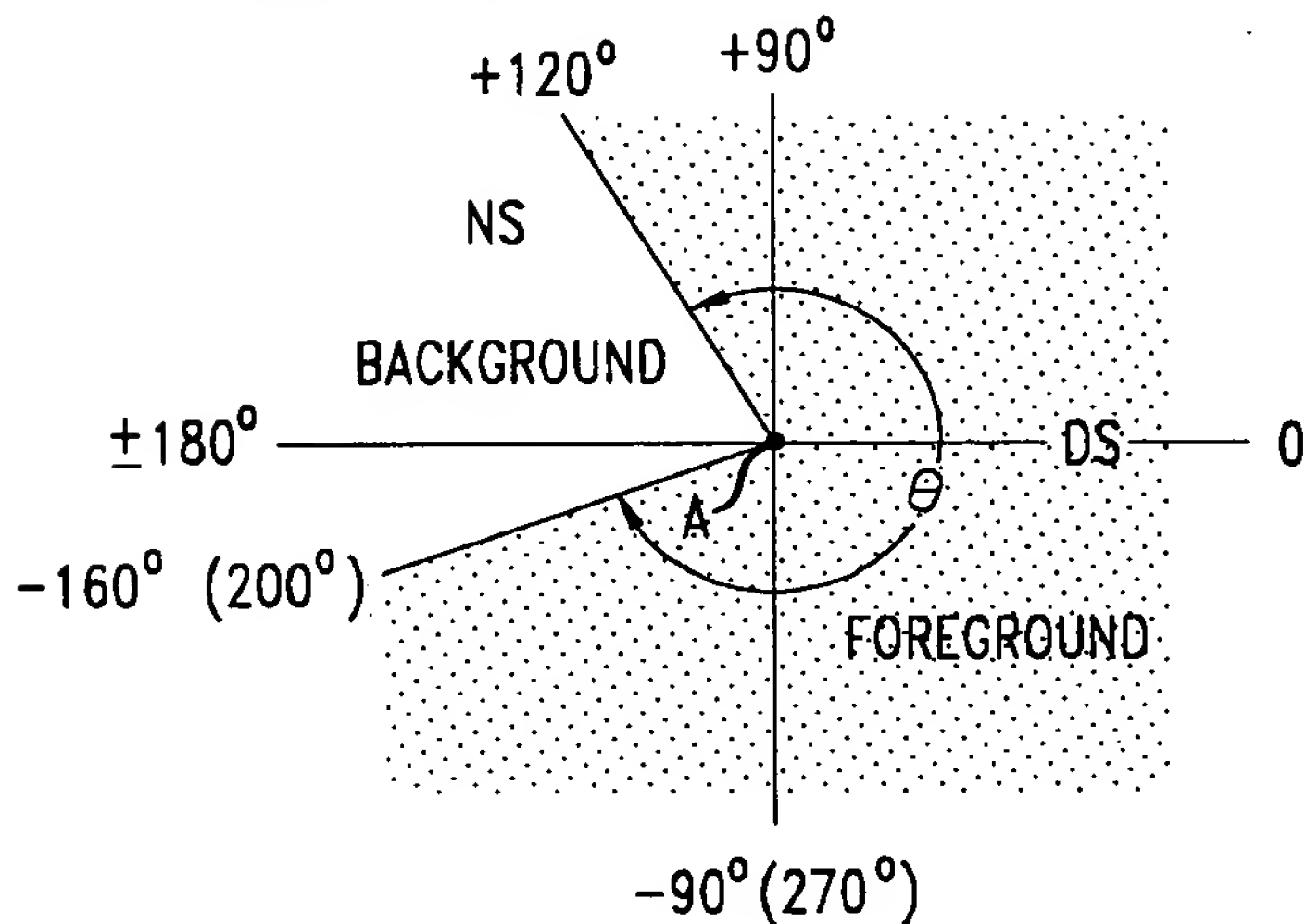


FIG. 1c



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O.G. FIG. 2,3	CLASS	38/92
	SUBCLASS	

FIG. 2

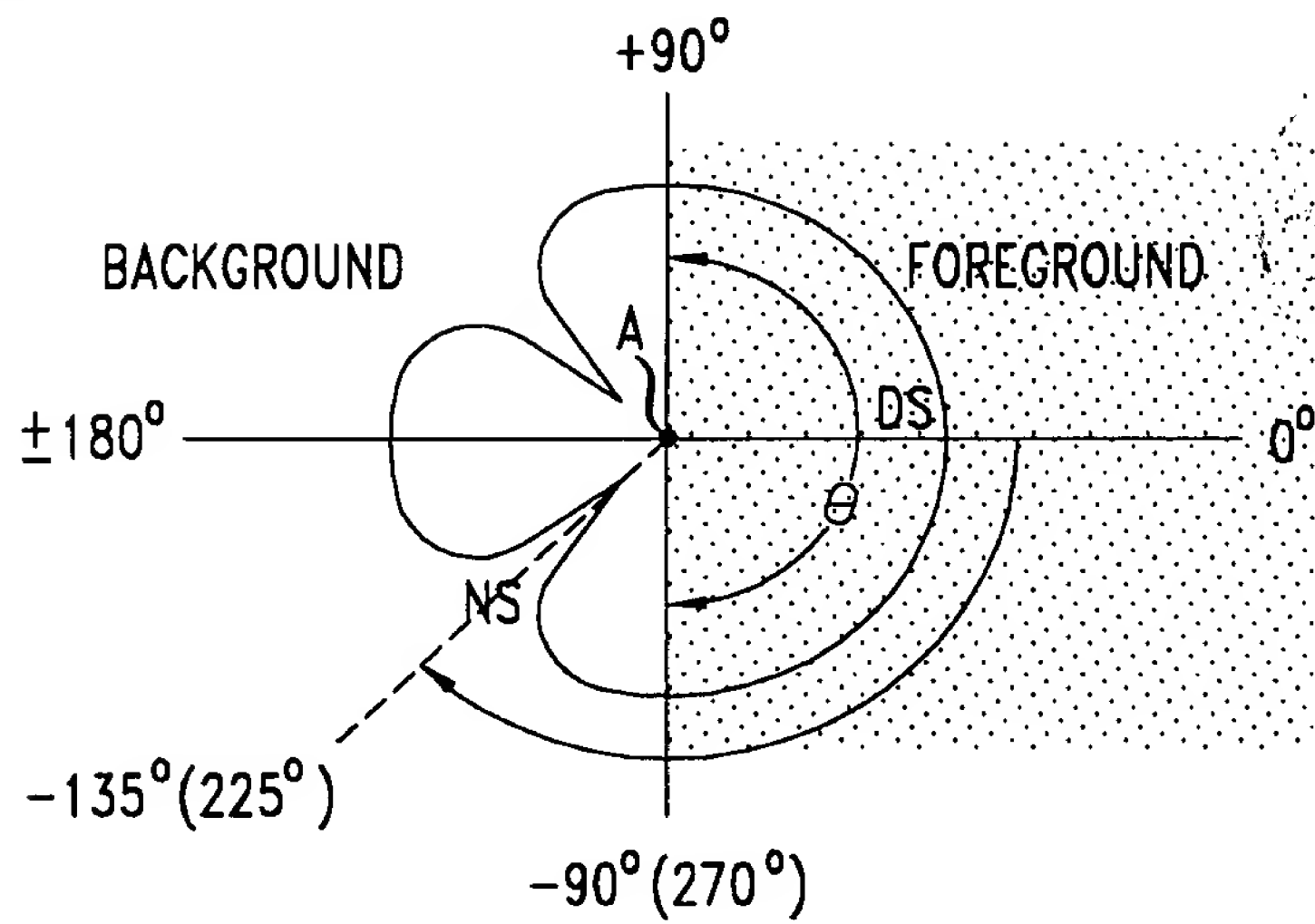


FIG. 3

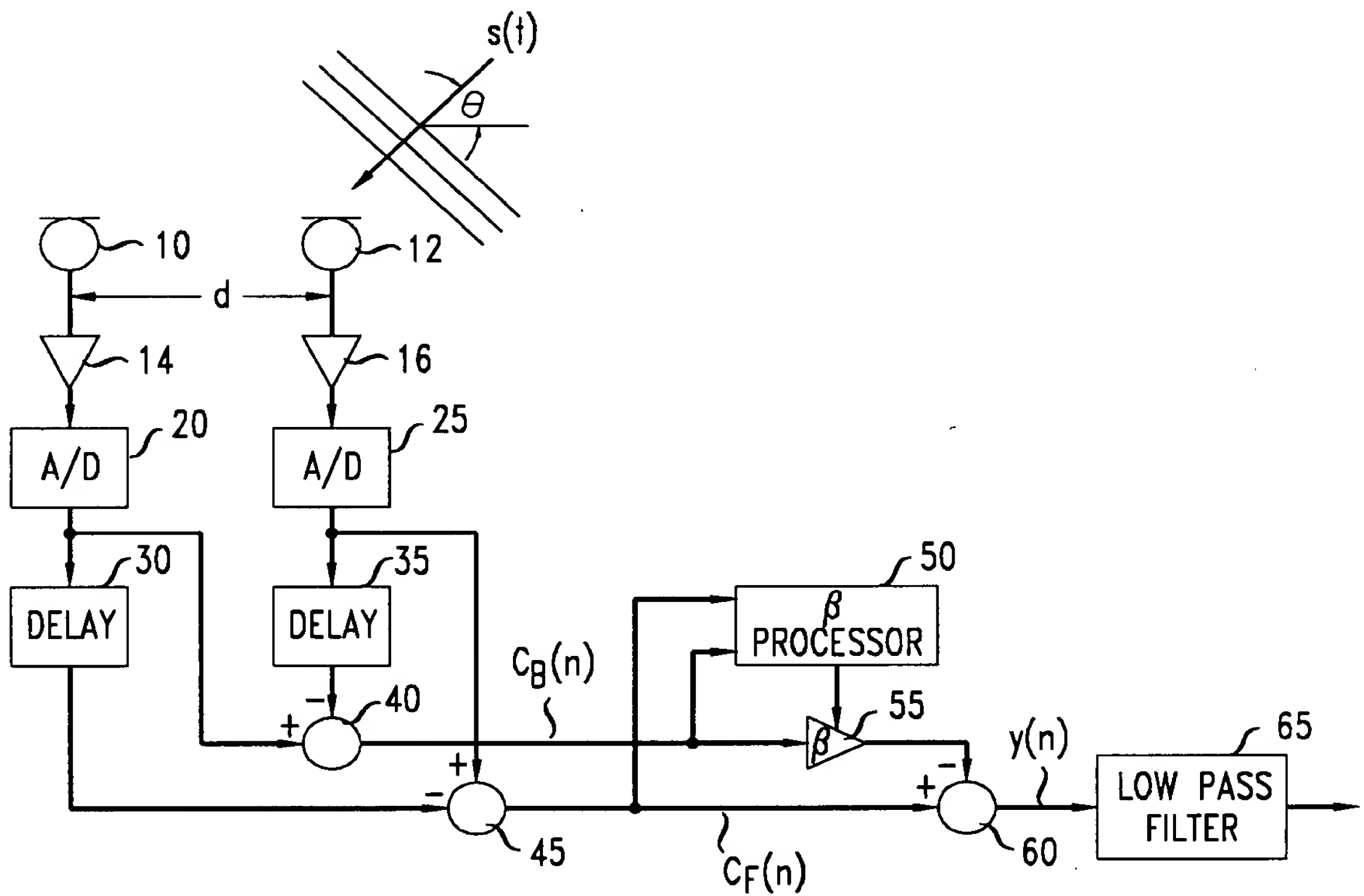


FIG. 4

O.G. FIG.	CLASS	SUBCLASS
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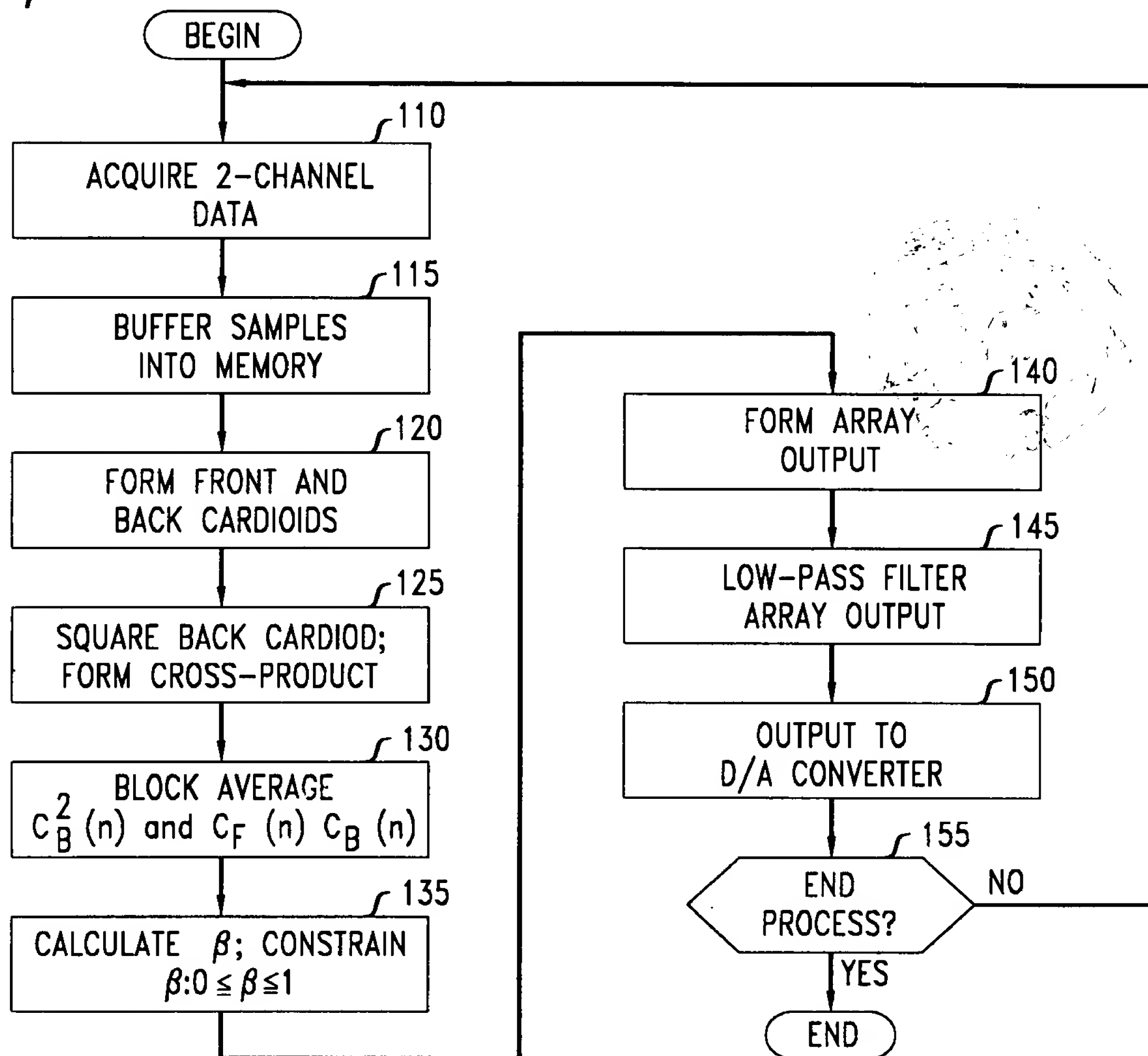
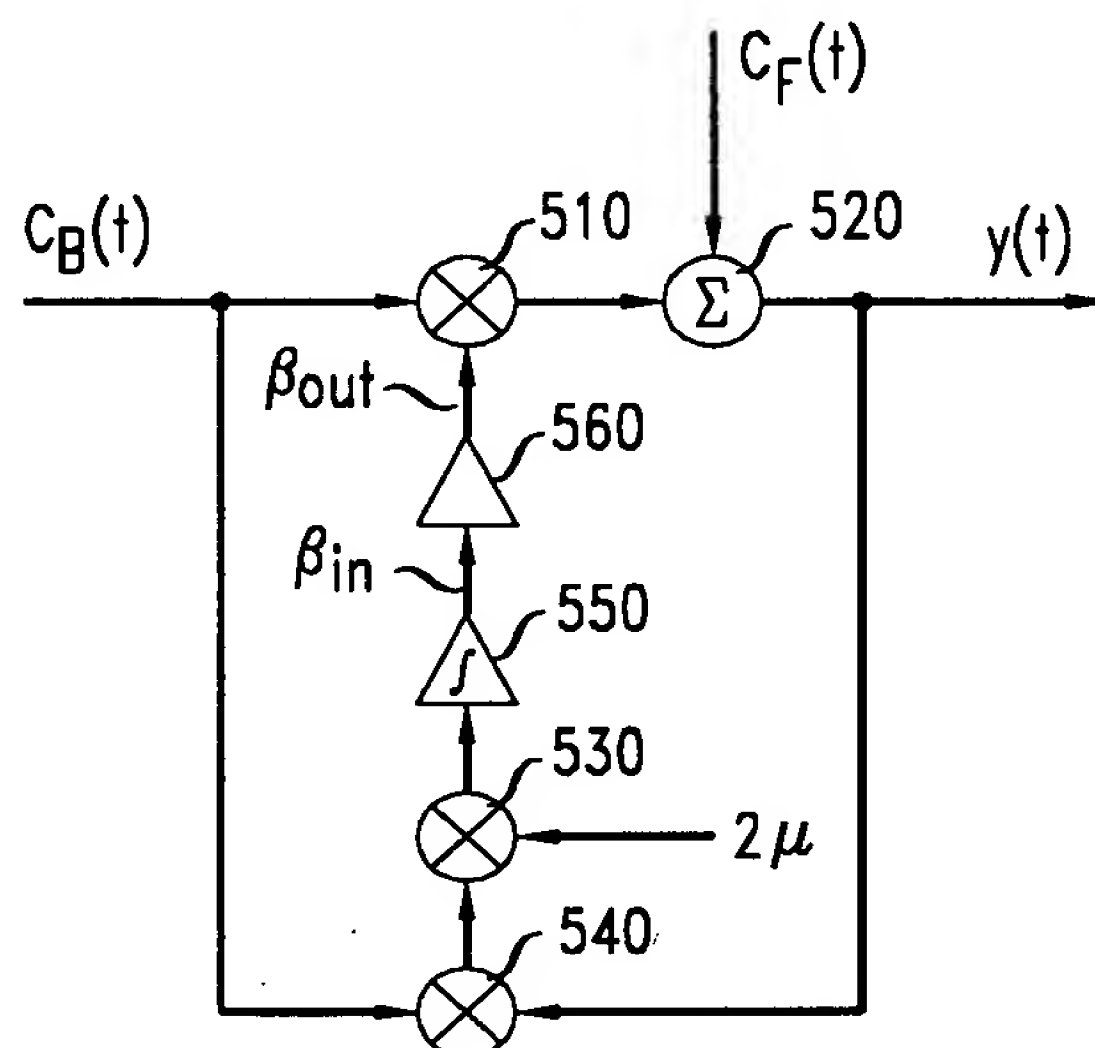


FIG. 5



6a

The circuit diagram shows an operational amplifier (op-amp) configured as a voltage follower (buffer). The non-inverting input (+) is connected to an input voltage  $V_i$ . The inverting input (-) is connected to the output  $V_o$ . A voltage divider is connected between  $V_o$  and ground, consisting of a resistor  $R_1$  in series with a variable resistor  $R_2$ . The output of the voltage divider,  $V_L$ , is connected back to the non-inverting input of the op-amp. The maximum voltage of the divider is  $V_{max}$ . The output voltage  $V_L$  is given by the formula:

$$V_L = \frac{R_2}{R_1 + R_2} V_{max}$$

A graph showing the relationship between  $\beta_{out}$  (vertical axis) and  $\beta_{in}$  (horizontal axis). The curve starts at the origin, rises linearly at a  $45^\circ$  angle, and then levels off to a constant value  $\beta_{out} = V_L$ .

The diagram illustrates a feedback system. An input signal enters a summing junction 40, where a feedback signal is subtracted. The output of junction 40 is the error signal  $C_B(n)$ . This signal is fed into a block labeled  $\beta$  PROCESSOR 220. The processor has multiple outputs:  $\beta_M/2$ ,  $\beta_1$ , and  $\beta_0$ . The error signal  $C_B(n)$  is also fed into a block labeled FB 215. The output of the FB block is fed into three multipliers 225, 226, and 227. The outputs of these multipliers are summed at junction 230. The output of junction 230 is fed into a summing junction 235, where the output of the DELAY block 210 is added. The final output of the system is  $y(n)$ .

FIG. 8

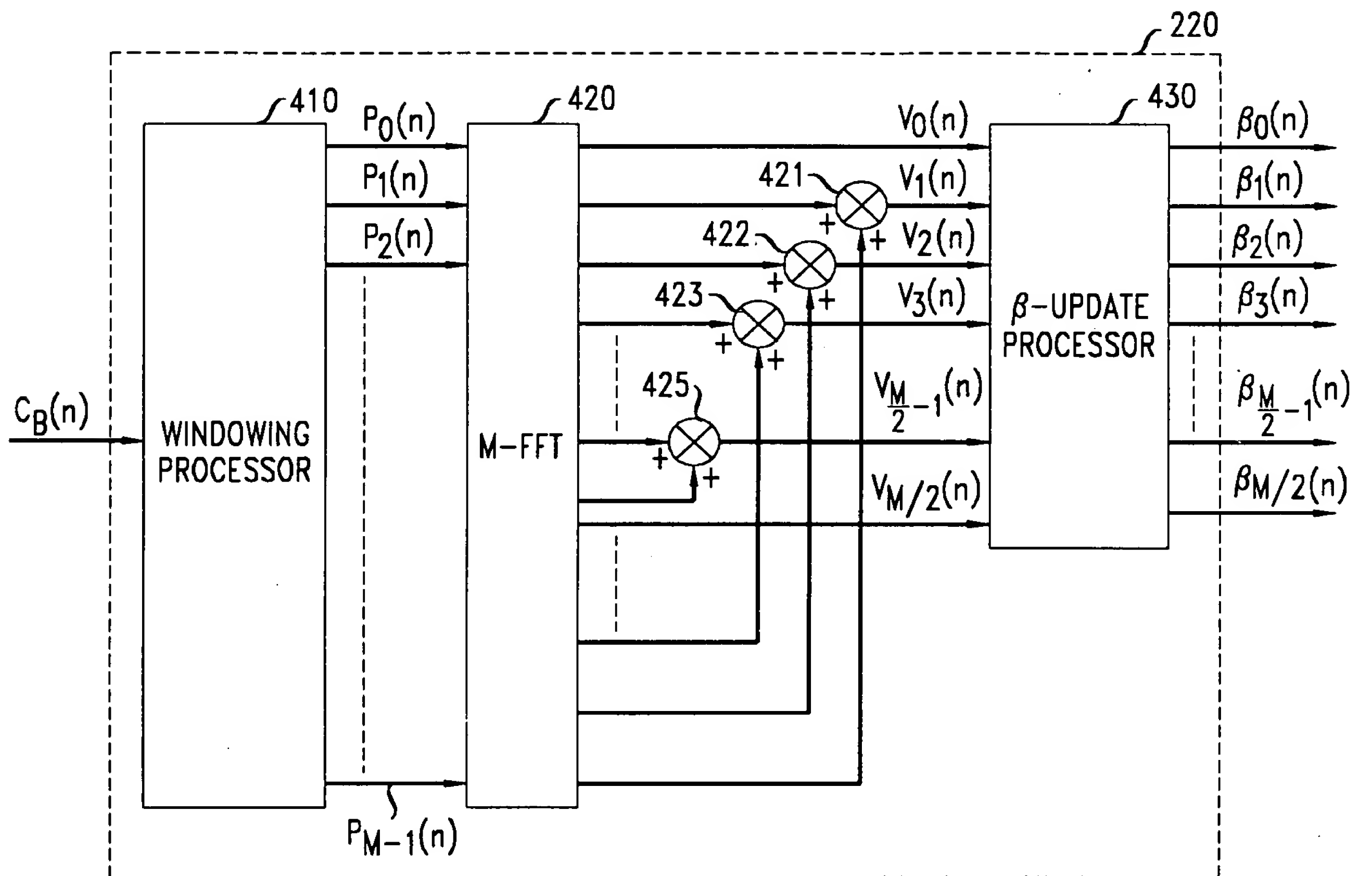


FIG. 9

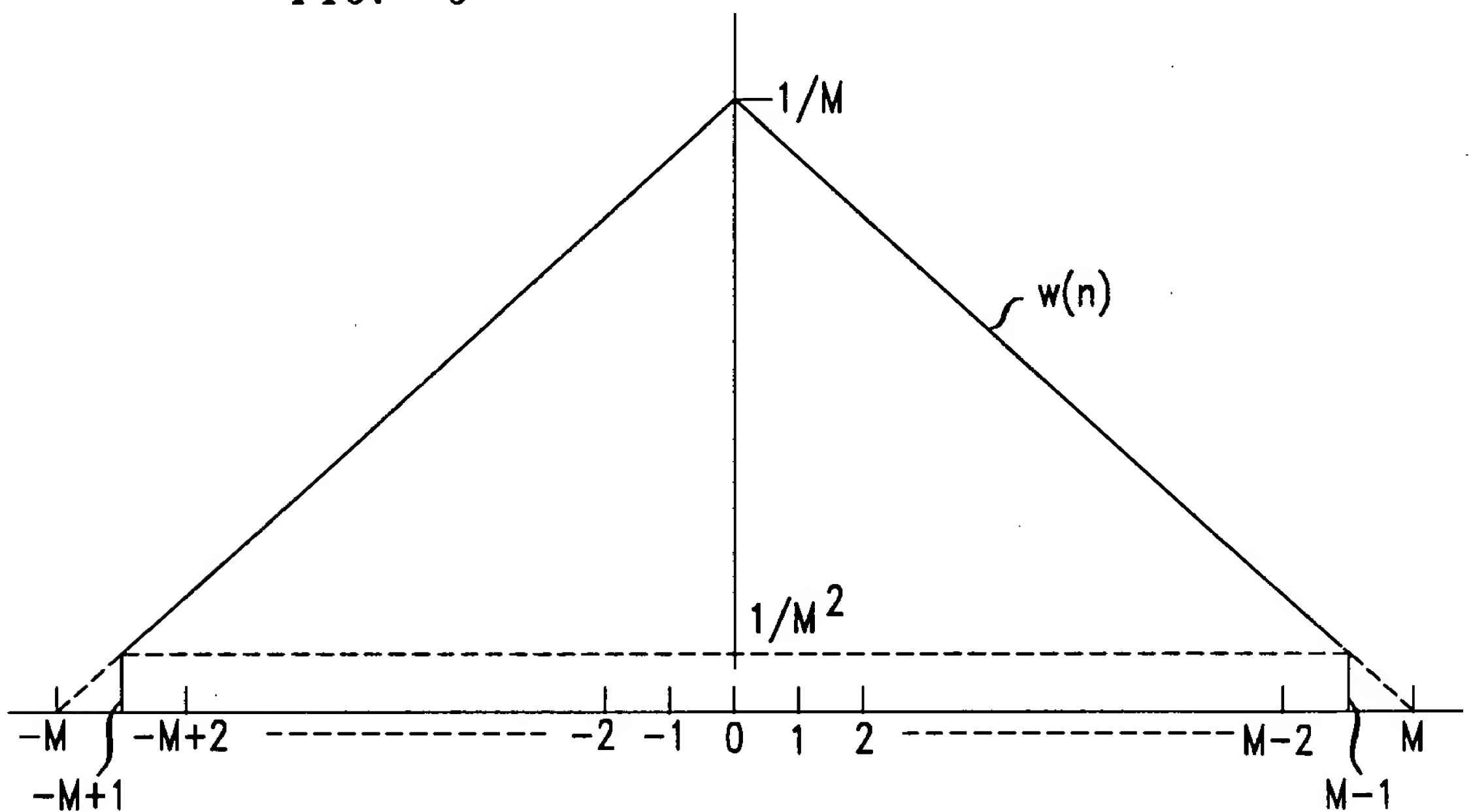


FIG. 10

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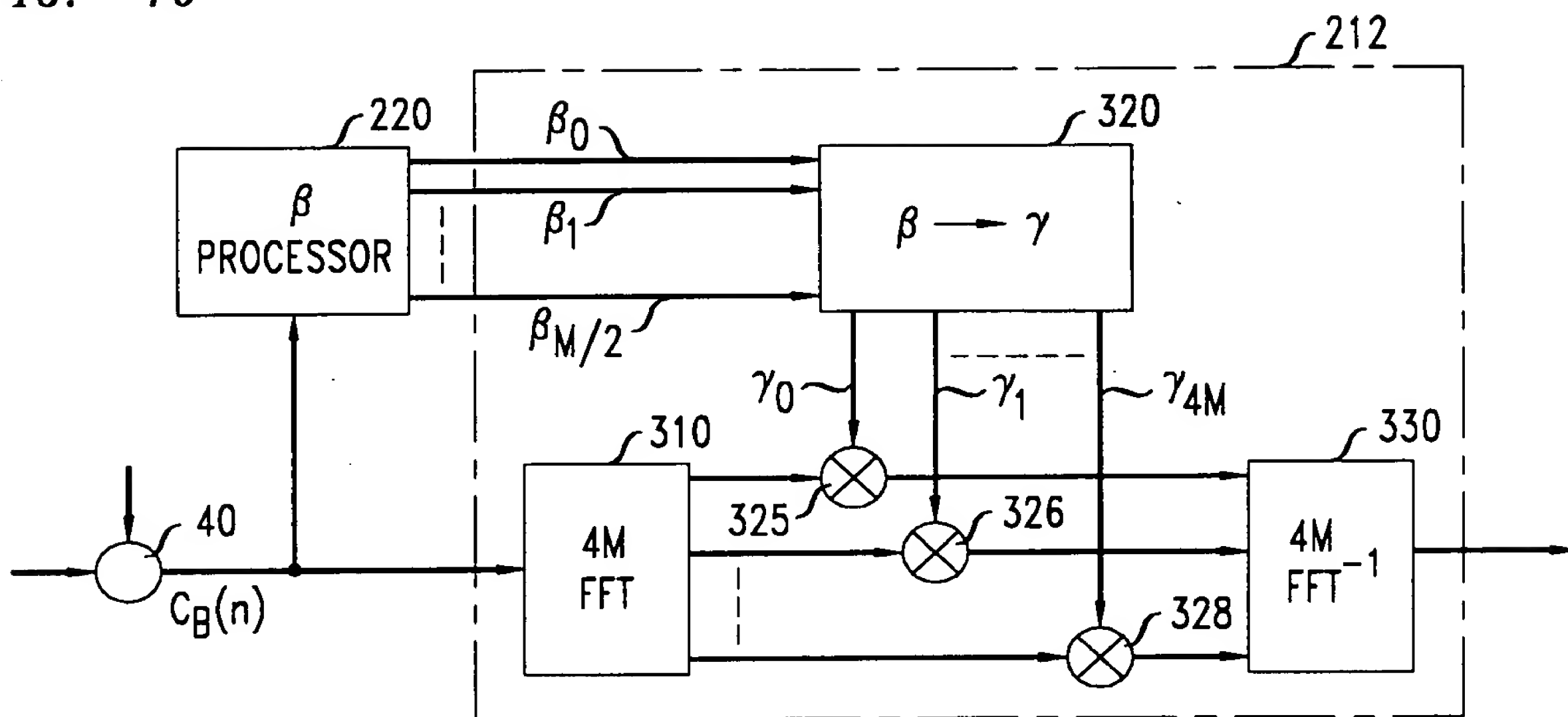


FIG. 11

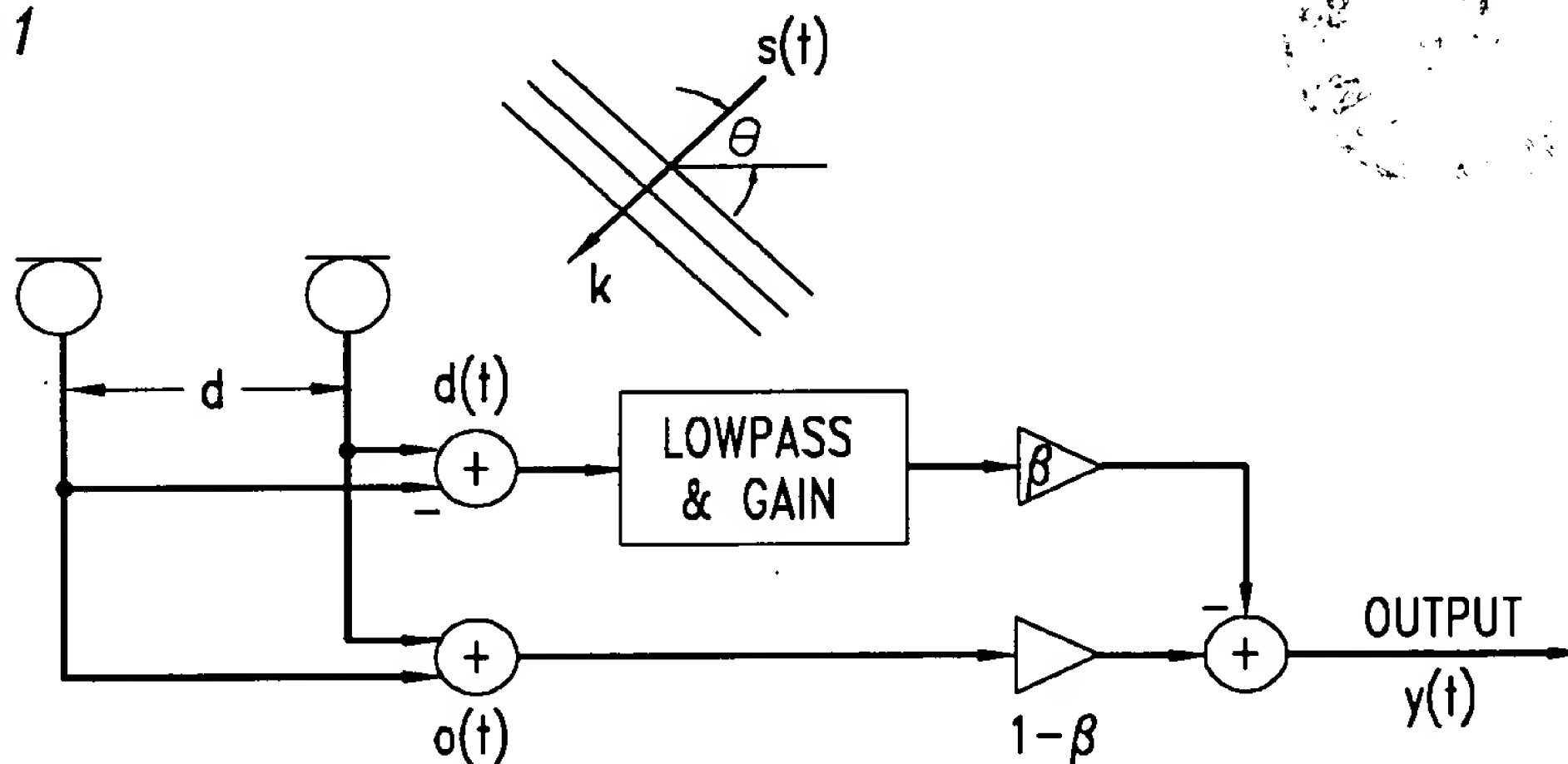


FIG. 12

